

Unleash image sensor dataflows

Engineered at intoPIX, TicoRAW is an innovative, lossless quality, low-power, low-memory and line-based image processing and compression technology created to unleash image sensor dataflows.

Thanks to its innovative processing and coding, the full power of the image sensor is preserved while reducing the bandwidth and storage needs. It offers high image quality and the capability to manage high resolution, high frame rate and high dynamic range workflows. TicoRAW is the world's first codec that can offer compression efficiency with such low complexity.

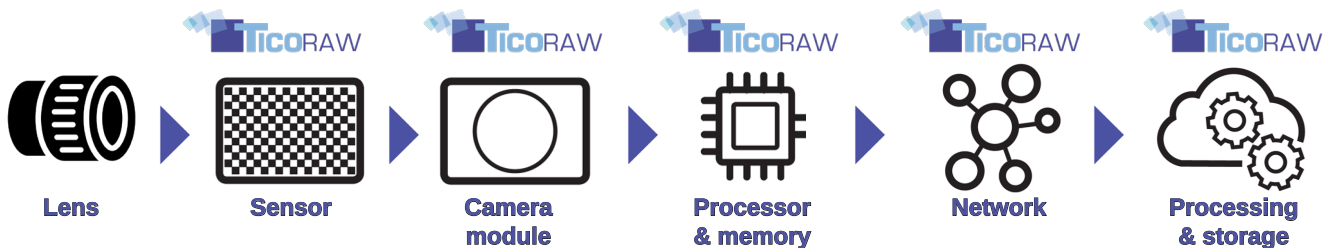
TicoRAW is a perfect solution for XR, medical, automotive (ADAS), human and machine vision, professional and consumer cameras (stills and videos), drones or mobiles devices. The technology is extremely low-power and tiny in ASIC or FPGA, fast and powerful in CPU or GPU, and suitable for latency-critical environments.



Technology benefits

- > High quality RAW
 - Supports image sensors up to 16bit; with High Dynamic Range (HDR)
 - Compresses down to 1 bit per pixel (2:1 to 16:1)
 - Perfect for human and machine vision
- > From 1 megapixel to 200 megapixels
 - Includes embedded proxy decoding mode
- > FPGA & ASIC IP-cores
 - Extremely low resource usage, low-memory, low-power
 - Microsecond line-based latency
- > Developer SDK for CPU & GPU
 - Powerful, real-time or faster than real-time

Where can TicoRAW be implemented?



- Reduce your power consumption. Process and manage more pixels from the sensor.
- Reduce your bandwidth during real-time transmission over network infrastructures without affecting the latency.
- Support higher resolution, high frame rate and high dynamic range easily.
- Reduce your memory bandwidth in the image processing pipeline (ISP).
- Efficiently decrease the stored RAW image data on the storage media. (RAW 10x smaller)
- Increase your decoding speed while retaining the sensor data needed for a complete control of the RAW processing pipeline.

Specifications and implementations

| TicoRAW ENCODER & DECODER | | |
|---------------------------|---------------------------------|---|
| IMAGE/VIDEO | Color Filter Array (CFA) | Bayer (RGGB, ...) and other RAW CFA such as RCCB, RYYCy, ... (Optional grayscale and 4:2:2 modes) |
| | Bit depth | 8 / 10 / 12 / 14/ 16 bits per component |
| | Resolution | Any up to 20.480 x 10.240 pixels |
| | Frame rates | Any (depending on ASIC / FPGA IP-core or Developer SDK configuration) |
| PROCESSING | Quality | Mathematically lossless / Near-lossless / Visually lossless / Lossy down to 1bpp |
| | Rate control | CBR (constant bit rate) operation (optional Constant Quality mode) Adjustable down to 1bpp (~10:1) |
| | Latency | (Sub) Intra-frame: down to 0.1 millisecond |
| | Proxy mode | Downscaler in TicoRAW decoder for fast analysis, proxy viewing & editing |

| | TicoRAW IP-cores | FastTicoRAW SDK |
|-----------------------|---|--|
| IMPLEMENTATION | Platform | GPU: x86-64 Intel CPU OS: Windows, Linux, macOS |
| | Low complexity & fast processing | Highly parallelized GPU SDK processing Compatible CPU SDK (SSE 4.1 or newer) |
| | Real-time operation | Line-based latency (< 1 millisecond) < 1 frame |

IP-core releases

| IP-CORES -ENC / -DEC | Color sampling | Sensor bit depth | Resolution examples | Max frames per sec. | | |
|---|-------------------|---------------------|------------------------|---------------------|----------------|----------------|
| | | | | at 100 MHz* | at 250 MHz* | at 300 MHz* |
| IPX-TICO-RAW-2K (Up to 2048-pixels width) | RAW CFA | 8, 10, 12, | 2048 X 1080 | 335 | 839 | 1006 |
| | Bayer | 14, 16 | 2048 X 2048 | 177 | 442 | 530 |
| IPX-TICO-RAW-4K (Up to 4096-pixels width) | RAW CFA | 8, 10, 12, | 4096 X 2160 | 84 | 209 | 250 |
| | Bayer | 14, 16 | 4096 X 4096 | 44 | 110 | 132 |
| IPX-TICO-RAW-8K (Up to 8192-pixels width) | RAW CFA | 8, 10, 12, | 7680 X 4000 | 60 | 60 | 72 |
| | Bayer | 14, 16 | 8192 X 4320 | 21 | 52 | 62 |
| | | | 8192 X 8192 | 11 | 28 | 33 |

CONTACT INTOPIX FOR YOUR OWN CUSTOM IP-CORE & SDK CONFIGURATION

* Max Frequency (MHz) of the IP-cores can be adjusted according to your selected pixel per clock architecture and your targeted FPGA

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